

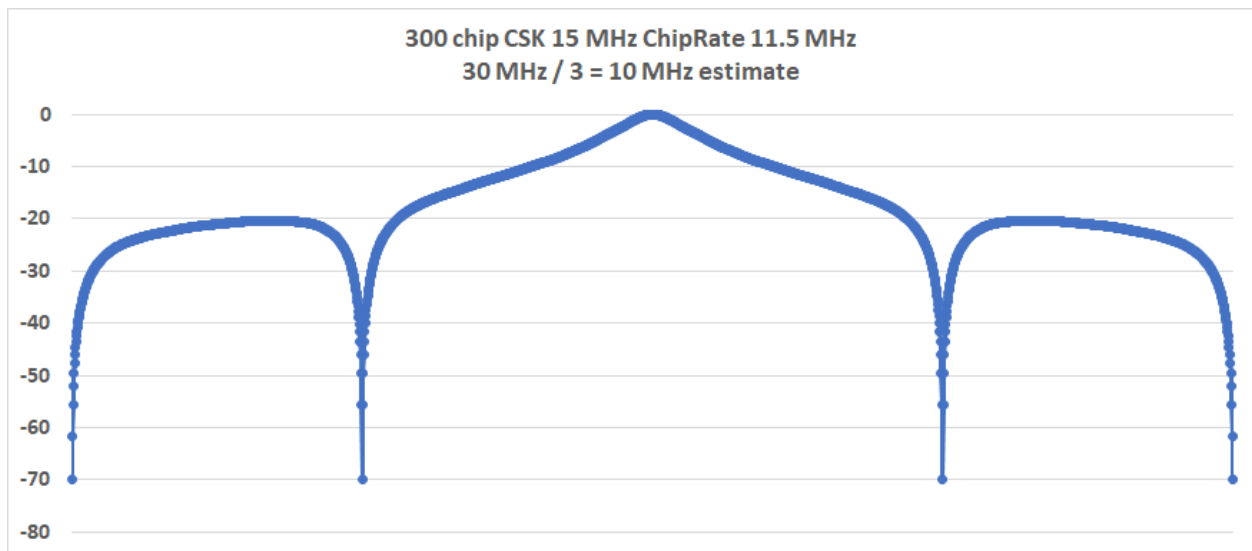


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The Specific Power Spectral Density Of The CSK 300-Chip CSK Code

The worst-case power spectral density profile of CSK Codes is shown in the figure at about -21 dB. Shift register PN codes all have a 1st sidelobe power spectral density peak of -18.81 dB relative to the peak of the Main Lobe. This side lobe level has plagued the shift register base codes bandwidth “extreme protection” criteria for the last 50 years. The CSK code generator configured for DPof2D binary code generation creates bandwidth-controlled CSK Codes -10 dB bandwidths of 2/3 chipping rate which reduces the 1st sidelobe peak to as low as -22.86 dB below main lobe peak Power Spectral Density.

This Paper presents the detail Power Spectral Density profile example verifying the general -10 dB bandwidth points estimated for the CSK Code. In the general CSK Code Null-to-Null is 2 * Chipping Rate. This figure estimated CSK Bandwidth is 2/3 Chip Rate (about 10 MHz). This rule of thumb was used as the estimate of any bandwidth from the known CSK Code length and family (DPof2PW or FCPW). The actual



CSK Code power spectral density for length 300 calculated DB scale has this BW of 11.5 MHz with sidelobe still about -21 dB below main lobe peak normalized power density at 0 dB. Of special interest is the smooth nature of the profile which indicates a stable random binary CSK code family. The spectral density parameters include .025 MHz frequency steps in the $(\text{SIN } X/X)^2$ profile calculated. The sidelobe peaks are 3 to 5 dB below the shift-register based codes such as used in GPS, GLONAS, Galileo.

Primary CSK Codes Advantages

- The FCPWD power spectral density profile shows the maximum 1st sidelobe peak of -21 dB
- The estimated FCPWD 1st sidelobe peak estimate is null-to-null / 3 = 10 MHz
- The calculated FCPWD power spectral density -10 dB bandwidth is 11.5 MHz
- The remaining sidelobe peaks for FCPWD are 3 to 5 dB below 1st sidelobe peak